1 Features

- Dual Channel, high Dynamic Range, fully differential audio mic/line AFE
- SPI controlled, fully integrated adjustable gain/attenuation
- -131dBU EIN (A-weighted, Rs = 0Ohm, +47dB gain)
- -18dB to +47dB Gain, 1dB steps
- High CMRR: 90dB typ. at 1KHz, gain = 0dB
- Accepts High Input levels: +28.7dBU balanced, +22.7dBU single-ended
- SPI Controlled Gain Steps (1dB)
- Optimized for 2Vrms (or 3Vrms) output ADC drive. Voltage centering option for DC coupling with ADC
- Flexible, SPI controlled GPIO pins for external input pad, HP filter, 48V phantom power switching, etc.
- Zero-Crossing Detect and DC servo for click/zipper free gain changes, user adjustable
- 7x7mm QFN 48 package
- Power supplies
  - Analog: +/-15V, +3.3V typ.
  - Digital +3.3V typ.

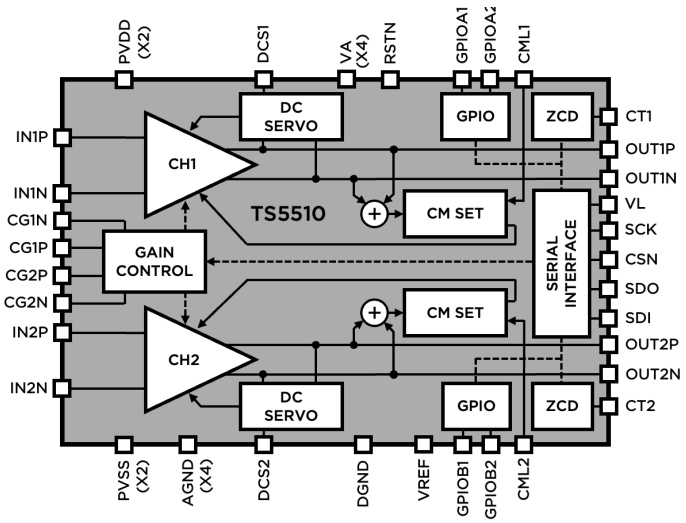
2 Applications

- USB Audio Interfaces
- Professional Audio Mixing Consoles
- Microphone Preamplifiers
- Stage Box / Audio Routers
- Remote Audio Installation

3 Description

Triad's TS5510 two channel, Low Noise Programmable Gain Input Amplifier is an audio analog front-end (AFE) for both modern at-home recording and professional mixing console applications. This innovative solution boasts an optimized gain topology, capable of matching both high and low-level audio signal inputs to contemporary audio ADCs, while preserving exceptional SNR throughout the gain range with flexible digital gain control, via an SPI interface. Control of the output voltage range and DC positioning allow direct connection to ADC inputs, reducing component count.

The TS5510 delivers high performance audio gain and attenuation level matching and SNR optimization in a small, easy to use QFN form-factor.



4 Device Overview

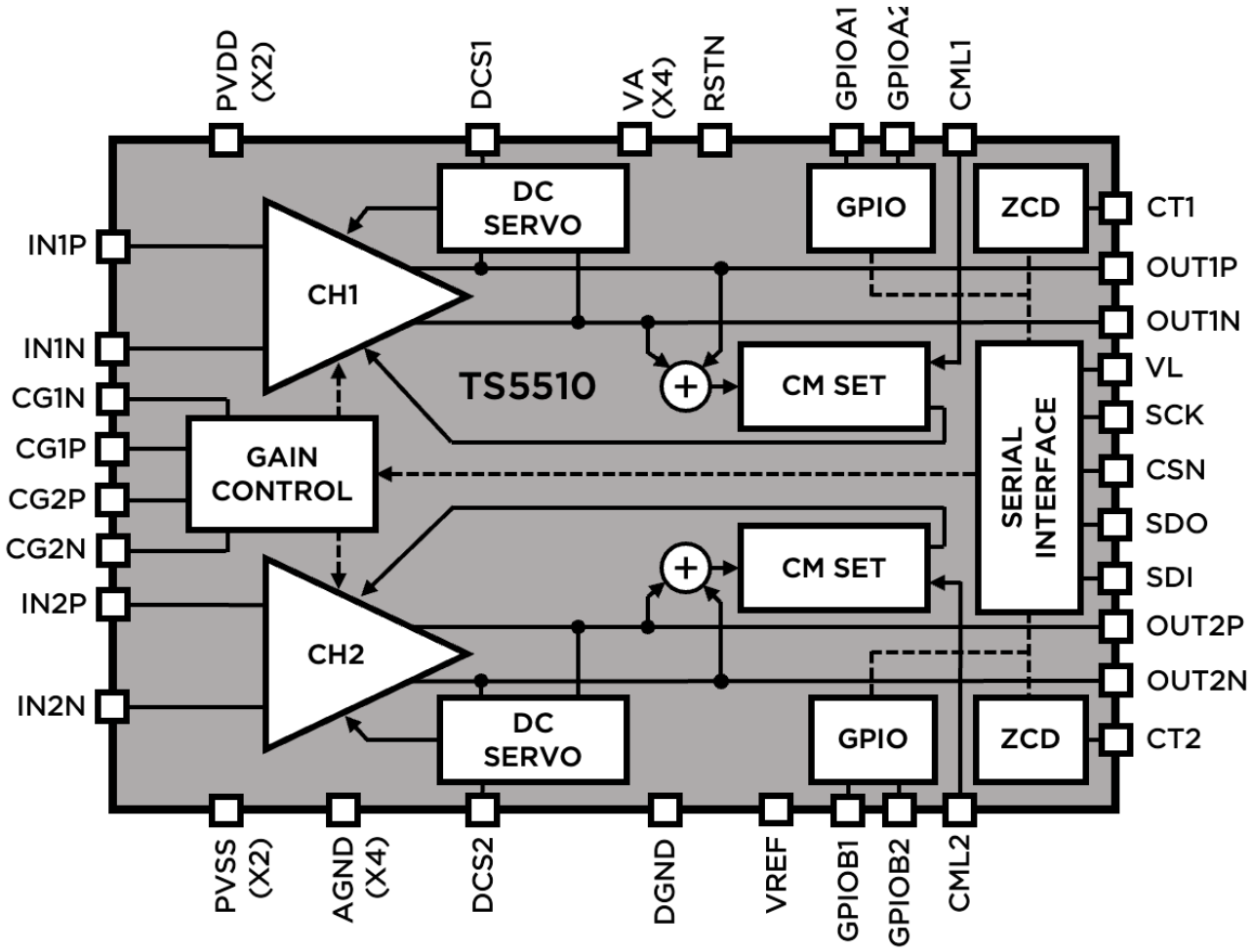


Figure 1: TS5510 Block Diagram

The Triad TS5510 is a two channel mic/line interface IC, designed to the basis of a flexible, digitally controlled AFE (Analog Front End) to a high performance digital audio ADC. The input stage features a novel architecture which optimizes performance in both gain and attenuation modes, eliminating the need for external pad circuitry. Gains are adjustable (per channel) in 1dB steps seamlessly from -18dB to +47dB. DC positioning and correction circuits remove offsets from the input devices, allowing the outputs to be DC coupled into the subsequent ADC, eliminating many support components in-system. All gains and operational functionality are controlled from a SPI digital interface. Four GPIO pins are included allowing flexibility to configure the audio system in different ways: eg. controlling phantom power, driving LEDs or enabling high-pass filter circuits. ZCD (Zero Cross Detection) circuits are available on each channel to time gain switching events to minimize transients and "zipper" noise on sequential gain changes. Both software register settings & external component value options are available to optimize ZCD timeouts. ACTIVE, MUTE and SHUTDOWN operational modes are controlled by the SPI interface. The main analog power rails can operate from +/-6V up to +/-18V, and the output stage amplifier can be powered from +3.3V up to 5V (to suit the ADC chosen). The digital logic interface can operate from 3.3V down to 1.8V.

5 Performance Characteristics

5.1 Absolute Maximum Ratings

Parameter [1,2]	Notes/Conditions	MIN	MAX	units
PVDD	Analog Supply voltage	-0.3	20	V
PVSS	Analog Supply voltage	-0.3	-20	V
VA	Analog Supply voltage	-0.3	+5.5	V
VL	Logic Supply voltage	-0.3	+4	V
T_{STG}	Storage temperature	-55	150	°C
T_{JMAX}	Maximum junction temperature		125	°C
I_{SC}	Output short circuit to AGND	continuous		-
ESD_{HBM}	Electrostatic discharge voltage rating – human body model (absolute value, all except CGx pins)	+/-2		kV
$ESD_{HBM:CGx}$	Electrostatic discharge voltage rating – human body model (absolute value, CGx pins)	+/-1		kV

(1) All Voltages are specified with respect to AGND = DGND = EP = 0Vdc

(2) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

5.2 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

Parameter	Notes/Conditions	MIN	TYP	MAX	units
PVDD / PVSS	Input Stage Supply voltage	+/-6	+/-15	+/-18	V
VA	Output Stage Supply voltage	+3.15	+3.3	+5.25	V
VL	Logic Supply voltage	+1.71	+1.8	+3.63	V
GND	AGND = DGND (connected on chip) = EP		0		V
T_{AMB}	Operating temperature range	-40		85	°C

5.3 Thermal Information

Parameter	Thermal Metric	QFN-48	units
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	37	°C/W

5.4 Electrical Characteristics

(PVDD = +15V, PVSS = -15V, VA = +3.3V, VL = +1.8V, AGND = DGND = 0V, CDCSx = 4.7uF, CINxP = CINxN = 2.2uF, RINxP = RINxN = 5Kohm to AGND, CGx = 330uF, CTx = 100nF, CCMLx = 4.7uF, CSDO = 10pF. Exposed Pad = 0V. Rload = 5K to AGND, each leg. Gain setting = 0dB *(note 1)*. Ambient temp = +27degC unless otherwise noted)

Parameter	Symbol	Conditions	MIN	TYP	MAX	units
DC Characteristics						
Undervoltage Lockout	V_{UVLO}	VL falling	1.62		1.70	V
UVLO Hysteresis (VL)	V_{HYS}			35		mV
Quiescent Supply Current	I_{PVDD}	Normal Operation (per channel)		9	13	mA
	I_{PVSS}		-13	-9		mA
	I_{VA}			11.3	15	mA
	I_{VL}	Normal Operation			1.2	mA
	I_{PVDD}	Shutdown		200		uA
	I_{PVSS}			400		uA
	I_{VA}			300		uA
	I_{VL}			75		uA
CMLx to OUTx DC Error	V_{CMOS}	CMLx input vs. (OUTxP + OUTxN)/2		0	+/-5	mV
Common Mode Reference Input Range	V_{CMLx}	At CMLx pin	1.55		VA-1.55	V
Common Mode Reference Input Impedance	R_{CMLx}		85	120		Kohm
Differential DC Output Offset	V_{OS}			0	+/-5	mV
SIGNAL GAIN						
Gain Range			-18		47	dB
Step Size				1		dB
Adjacent Gain Step Error		*(note 2)*			+/-0.2	dB
Gain Accuracy at 0dB Setting			-0.1		+0.35	dB
Mute Attenuation		0dB, fin = 1KHz		100		dB
INPUT						
CMRR	CMRR	fin = 1KHz, Vin = 1Vrms common mode		90		dB
Common Mode Input Range	CMR	INxP = INxN	PVSS + 2.5		PVDD – 2.0	V
Input Impedance	R_{IN}	At 1KHz, Differential	1			Mohm
Input Referred Noise	EIN_A	A-weighted, Rs = 0, Gain = 47dB		-131		dBU
	EIN_{UN}	20Hz-20KHz, Rs = 0, Gain = 47dB		-128		dBU
1/f Noise Corner		+3dB w.r.t. flat noise floor, Gain = 47dB		200		Hz

(PVDD = +15V, PVSS = -15V, VA = +3.3V, VL = +1.8V, AGND = DGND = 0V, CDCSx = 4.7uF, CINxP = CINxN = 2.2uF, RINxP = RINxN = 5Kohm to AGND, CGx = 330uF, CTx = 100nF, CCMLx = 4.7uF, CSDO = 10pF. Exposed Pad = 0V. Rload = 5K to AGND, each leg. Gain setting = 0dB *(note 1)*. Ambient temp = +27degC unless otherwise noted)

Parameter	Symbol	Conditions	MIN	TYP	MAX	units
AC CHARACTERISTICS						
Full Power Bandwidth	BW	Any Gain Setting, -1dB Full Scale Out		40		KHz
Distortion	THD+N	fin = 1KHz, 1Vrms, 0dB gain		0.002		%
Click/pop on gain change	Kcp	A-weighted, peak reading, any 1dB gain step below 20dB, inputs shorted		-60		dBV
DC servo -3dB point		C_{DCS} = 4.7uF		0.025		Hz
Output Slew Rate	SR	5.6Vpp output	0.7			V/us
Rated Output Load Capacitance	C_{TYP}	22ohms + C_{TYP} + 22ohms across outputs			15	nF
Capacitive Load Stability	C_{MAX}	No sustained oscillations, each output to AGND	200			pF
Crosstalk		Gain = 0dB, 2Vrms on driven channel, fin = 1KHz		110		dB
Power Supply Rejection Ratio	PSRR	Rin = 150ohms, 100mV ripple at 1KHz, PVDD / PVSS		95		dB
		Rin = 150ohms, 100mV ripple at 1KHz, VA with CMLx = 1.65V fixed		85		dB
ZERO CROSS DETECTION						
ZCD Threshold	ZCD_{THR}	Measured at Output		+/-10		mV
ZCD Timeout	ZCD_{TMR}	Gain change executed if no ZC event after time: *(note 3)*	4	6.7	100	ms
DIGITAL INPUTS / OUTPUTS						
Digital Inputs						
Input High Voltage	V_{IH}		0.75 x VL			V
Input Low Voltage	V_{IL}				0.25 x VL	V
Input Leakage Current	I_L			+/-1		uA
Input Capacitance	C_{IN}			5		pF
Digital Output (SDO)						
Source Current	I_{OH}			4		mA
Sink Current	I_{OL}			4		mA
Output Voltage High	V_{OH}	I_{SOURCE} = 4mA (VL = 3.3V)	0.9 x VL			V
Output Voltage Low	V_{OL}	I_{SINK} = 4mA (VL = 3.3V)			0.1 x VL	V
Digital Outputs (GPIO)						
Sink Current	I_{OL}			4		mA
Output Voltage Low	V_{OL}	I_{SINK} = 4mA (VL = 3.3V)			0.1 x VL	V
Pull up Resistance	R_{PU}	Internal, when GPIO set as input / high output (to VL)		8		Kohm

(PVDD = +15V, PVSS = -15V, VA = +3.3V, VL = +1.8V, AGND = DGND = 0V, CDCSx = 4.7uF, CINxP = CINxN = 2.2uF, RINxP = RINxN = 5Kohm to AGND, CGx = 330uF, CTx = 100nF, CCMLx = 4.7uF, CSDO = 10pF. Exposed Pad = 0V. Rload = 5K to AGND, each leg. Gain setting = 0dB *(note 1)*. Ambient temp = +27degC unless otherwise noted)

Parameter	Symbol	Conditions	MIN	TYP	MAX	units
DIGITAL INPUTS / OUTPUTS						
Reset Pin (RSTN)						
Output Voltage Low	V_{OL}	I_{SINK} = 4mA (VL = 3.3V)			0.1 x VL	V
Pull up Resistance	R_{PU}	*(note 4)*		320		Kohm
Sink Current	I_{OL}			4		mA
SPI INTERFACE TIMING						
Timing Characteristics (VL = 1.8V)						
SCK Frequency					4	MHz
SCK Clock Period	Tcp	Assumes rise/fall time < 10ns	250			ns
SCK Pulse Width High	Tch		105			ns
SCK Pulse Width Low	Tcl		105			ns
SCK Fall to SDO	Tdo		10		80	ns
CSN Fall to SCK Rise Setup	Tcss		70			ns
SCK Fall to CSN Rise Hold	Tcsh		70			ns
SDI to SCK Setup	Tds		60			ns
SCK Rise to SDI Hold	Tdh		60			ns
CSN Fall to SDO Delay	Tcsdo		0		80	ns
CSN Rise to SDO Hold	Tcsdh		0		80	ns
CSN Pulse Width High or Low	Tcsw	*(note 5)*	2			us
Timing Characteristics (VL = 3.3V)						
SCK Frequency					5	MHz
SCK Clock Period	Tcp	Assumes rise/fall time < 10ns	200			ns
SCK Pulse Width High	Tch		80			ns
SCK Pulse Width Low	Tcl		80			ns
SCK Fall to SDO	Tdo		5		50	ns
CSN Fall to SCK Rise Setup	Tcss		25			ns
SCK Fall to CSN Rise Hold	Tcsh		25			ns
SDI to SCK Setup	Tds		25			ns
SCK Rise to SDI Hold	Tdh		25			ns
CSN Fall to SDO Delay	Tcsdo		0		25	ns
CSN Rise to SDO Hold	Tcsdh		0		25	ns
CSN Pulse Width High or Low	Tcsw	*(note 5)*	2			us

Notes:

note 1: "Unity gain" internal setting is defined as V(OUTxP – OUTxN)/V(INxP - INxN) = 1 for AC (audio band) signals
note 2: This is the gain error from the expected 1dB when moving from one gain step to an adjacent setting, either higher or lower
note 3: power on default value, can be changed by SPI register write command. Settings can also be scaled by adjusting the value of CTx capacitors from nominal value
note 4: Note that the reset pin RSTN is actively driven low internally by the TS5510 until all supply rails are above the UVLO minimums. Forcing this pin low will reset the device control registers
note 5: This minimum time period is to allow internal status transfer between the asynchronous ZCD timer registers between CSN events

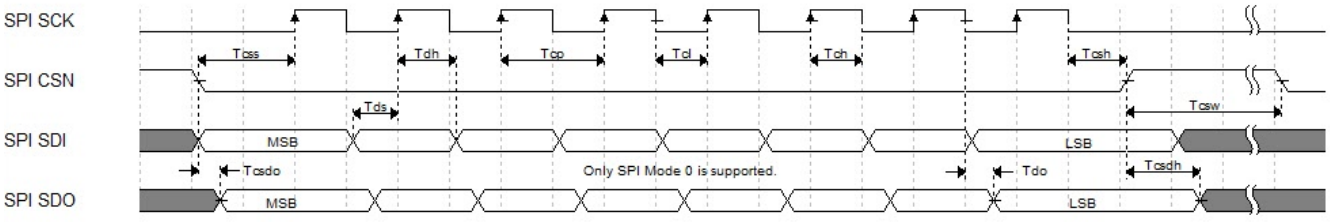


Figure 2: Timing Characteristics for SPI Interface (mode 0 only)

6 Typical Operating Characteristics

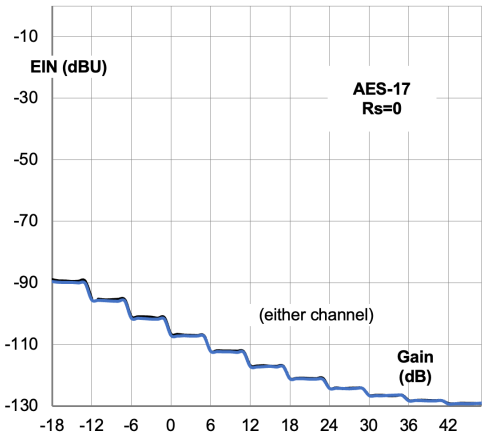


Figure 3.1: EIN (Equivalent Input Noise) vs. Gain

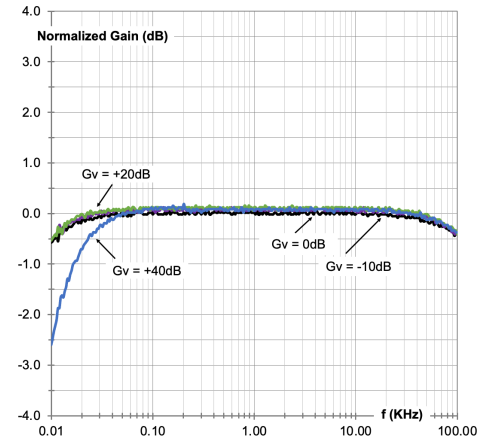


Figure 3.2: Normalized Gain vs. Frequency

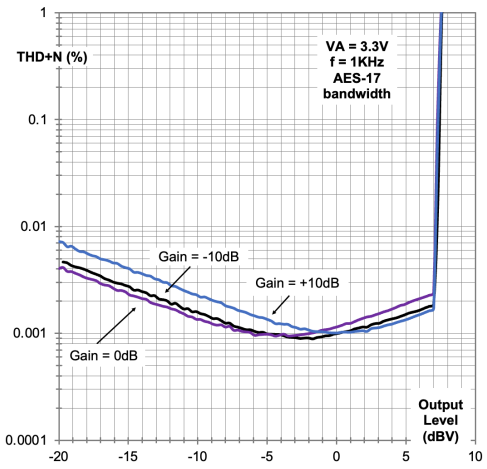


Figure 3.3: THD+N vs. Output Level

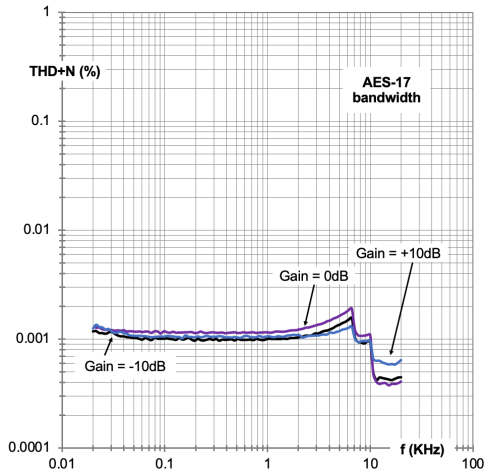


Figure 3.4: THD+N vs. Frequency (1Vrms out)

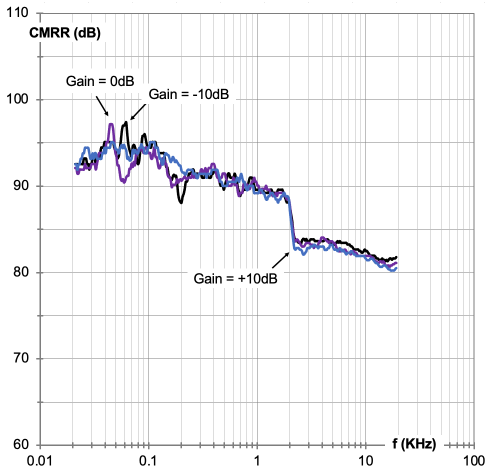


Figure 3.5: CMRR vs. Frequency

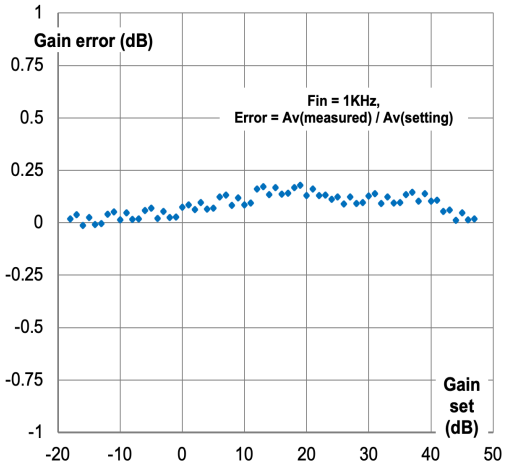


Figure 3.6: Overall Gain Error vs. Setting

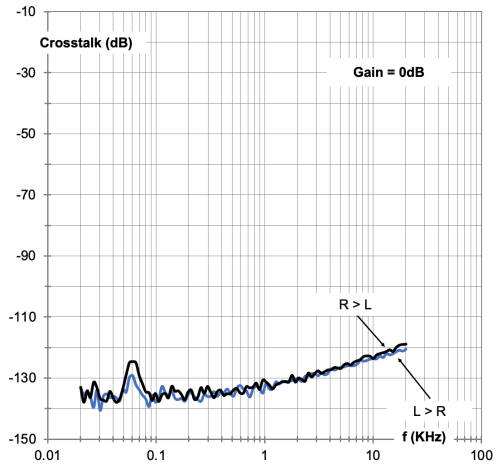


Figure 3.7: Crosstalk vs. Frequency

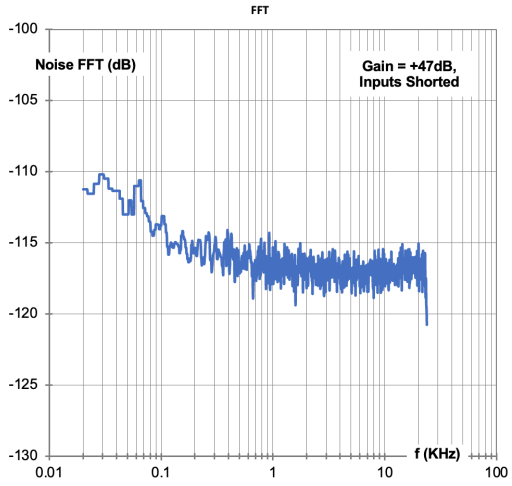


Figure 3.8: Noise Floor FFT Profile

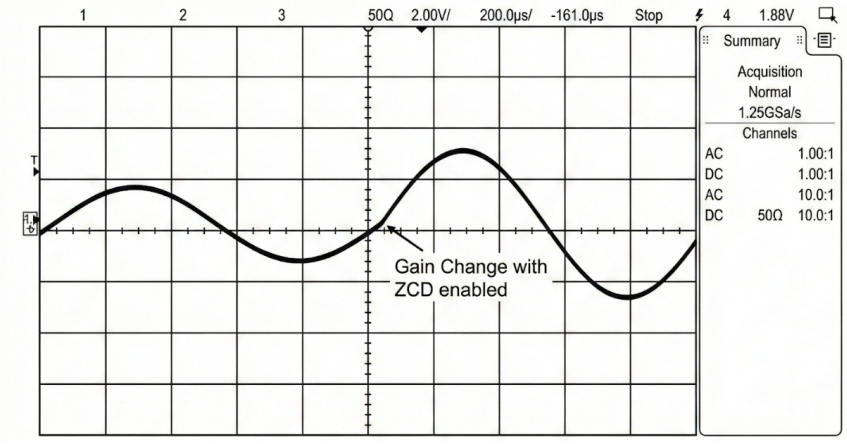


Figure 3.9: Gain Change Example – ZCD Enabled

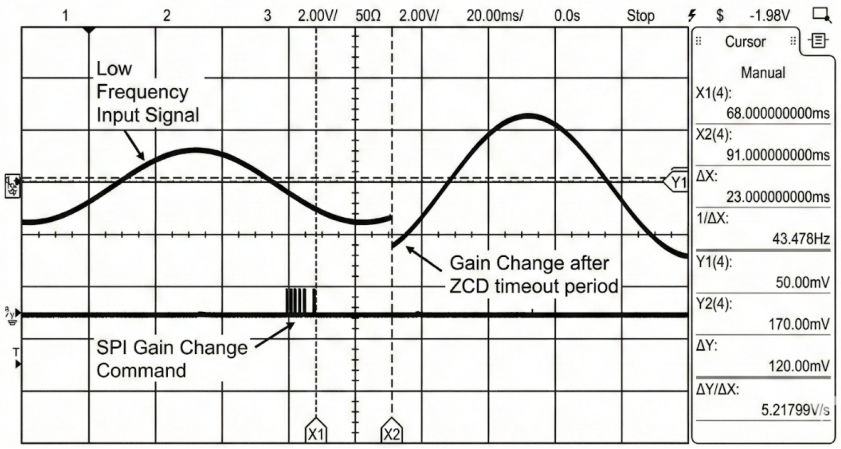


Figure 3.10: Gain Change Example Showing ZCD Timeout in the Presence of Low Frequency Input

7 Detailed Description

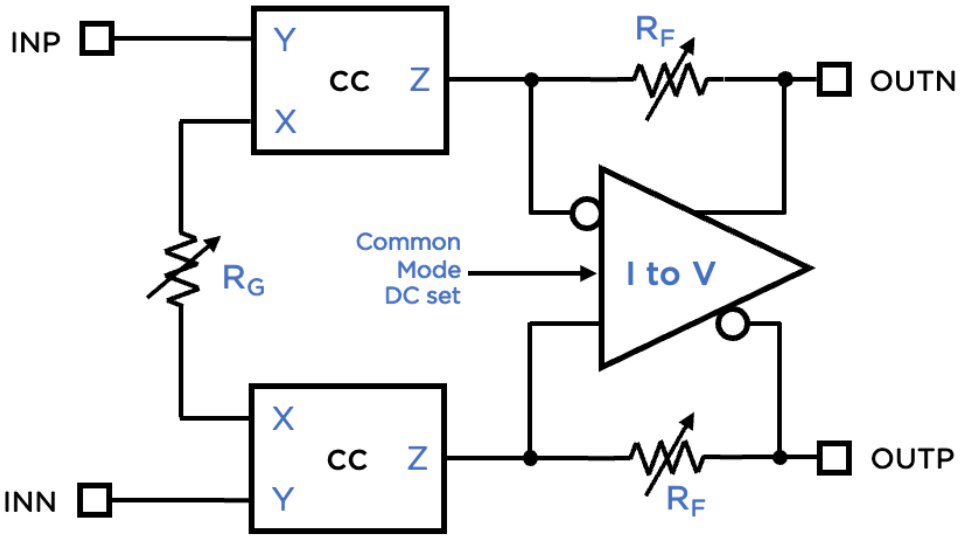


Figure 4: Simplified Amplifier Architecture, single channel shown

7.1 Amplifier Topology

The TS5510 is a high performance audio AFE (Analog Front End) which has been designed to optimize the capture of single-ended or differential audio analog inputs and provide a low impedance output drive at levels suitable for digital conversion by a contemporary stereo ADC. The seamless gain and attenuation modes can accommodate a wide range of input amplitudes, and the output DC control options minimize external passive components between the TS5510 and the subsequent stereo ADC.

Figure 4 shows a simplified overview of how the amplifier is configured internally. There are two stages of amplification:

- A first stage which is configured as a low noise, differential voltage to current (V to I) converter (dual Current Conveyors)
- A second stage which has a high current, low impedance output capability optimized to drive ADC inputs, configured as a current to voltage (I to V) converter

The 1st stage provides coarse gain steps, by using two ultra-low noise Current Conveyor amplifier blocks, whose current output (X terminals) is fed into a switched resistive ladder shared between the two Conveyors. The values of this resistive ladder are chosen to provide the 6dB "coarse" gain and attenuation steps, needed for all gain settings in the IC (R_G in Figure 4). A precision replica of the Current Conveyor output current (Z terminals) is fed forward to the second stage.

The second stage is configured as a conventional differential current to voltage (I to V) converter, translating the fed forward current from the first stage into a balanced output voltage. Fine gain steps are done in this 2nd stage, in 1dB increments, the full range available from this stage being 0 to +5dB.

The overall topology of the Current Conveyor-based input stages followed by the differential I to V stage has a number of key advantages over previous integrated AFE approaches:

Common Mode Rejection at the Input: Unlike a conventional Instrumentation Amplifier configuration, where the 1st stage acts as a follower to CM signals (requiring any subsequent stages to tolerate and/or reduce it), the TS5510 topology substantially eliminates any CM signals at the 1st stage (Current Conveyors). The fed forward replica current from the Conveyors contains no CM content, therefore the 2nd stage is operating purely on intended (differential) signal - not noise, hum or interference – much like using a transformer coupled input.

Internal and external optimized power rails: By design, the signal transfer between 1st and 2nd stages within the IC is in the current domain. These currents are fed to a differential "virtual earth" stage for voltage conversion which can be independently DC biased. This means there is a convenient "domain barrier" between the circuitry that handles the incoming signals and the output amplifier which drives the ADC input. The TS5510 input stage power pins (PVDD, PVSS) allow up to +/-18V rails to accommodate high level inputs signals without distortion or clipping, as well as being able to tolerate a high level of Common Mode signal (see later section on CMR).

The TS5510 output stage drive to the ADC only needs to support enough signal voltage headroom to drive the ADC to 0dBFS. Given that most modern stereo ADCs require either 3.3V or 5.0V analog rails for operation – and their inputs are typically biased to mid-rail – the 2nd stage of the TS5510 can conveniently be powered from the same rail as the ADC and dedicated bias pins (CMLx) allow DC positioning of the outputs to match the "center" input operating voltage inputs of the ADC. This means:

- The TS5510 output stage quiescent power is minimized, and not dependent on the input rail (high signal compliance) requirements. The 2nd stage can use the same "analog" supply rail as the ADC (pin VA on the TS5510). No negative rail is required for the TS5510 2nd stage
- Capacitive coupling between the TS5510 outputs and the ADC is no longer necessary. Note the inputs of the TS5510 still require capacitive coupling, and stereo audio ADCs typically have digital-side DC removal High-pass filters
- The TS5510 can never overload the ADC input circuitry (even when clipping), as both ICs are powered from the same rail. This eliminates the need for any overload protection circuitry on the ADC input

High Input Impedance: Many AFE input stages that are designed for low noise, typically use bipolar transistors on the front end to optimize performance. With such devices being biased at mA level collector currents to obtain low EIN (equivalent input noise), base current requirements (combined with the need for AC input coupling) mean that the resistors used to tie the inputs to AGND (and supply transistor base current) are limited in value to a few Kohm. While this is typically OK for microphones, a system requiring flexibility on the inputs (mic / instrument inputs for example, such as combination TRS/XLR sockets) needs much higher input impedance to work well. The TS5510 input design allows much higher input resistors to be used (hundreds of Kohm) if desired in-system, allowing instruments to be plugged directly in and decreasing the value and physical size of the input AC coupling capacitors.

7.2 Input Considerations

7.2.1 Phantom Power Application

Phantom power should be applied to the input side of the coupling capacitors that couple into the TS5510 INxN and INxP pins (C1-C4 on the Applications Diagram), not directly to the IC. These input pins are designed to be robust to ESD transients, but will require external protection components to prevent any transient overload (outside those safe conditions described in the Absolute Maximums section) from damaging the inputs; such as when the +48V of Phantom power is applied or removed abruptly. An example protection circuit providing clamping to the PVDD/PVSS rails is shown in the Application Diagram (Section 9). Note that careful component selection is critical when selecting these components to not compromise linearity when operating normally.

7.2.2 Common Mode Rejection

As noted, the Common Mode rejection of the TS5510 is inherently high through the device itself. Consideration of the external support components is key to optimizing CMRR across frequency. The high input impedance of the TS5510 inputs allows physically smaller AC coupling capacitors to be used, but the matching of these components can affect the extension of high CMRR at low frequencies. Either oversizing the capacitor values, or matching time constants through the INxN and INxP paths will extend CMRR in this region.

7.2.3 Common Mode Input Range

The TS5510 can accommodate a wide range of input signals, as well as tolerating – and rejecting – a high level of Common Mode interference superimposed on the desired audio. High input signal levels can be accommodated with the attenuation settings of the TS5510 (typically eliminating the need for any external resistive divider or "pad"), but the amount of input Common Mode tolerated does alter with gain setting. Figure 5 shows the interaction of output signal swing, gain setting and Common Mode Input levels tolerated:

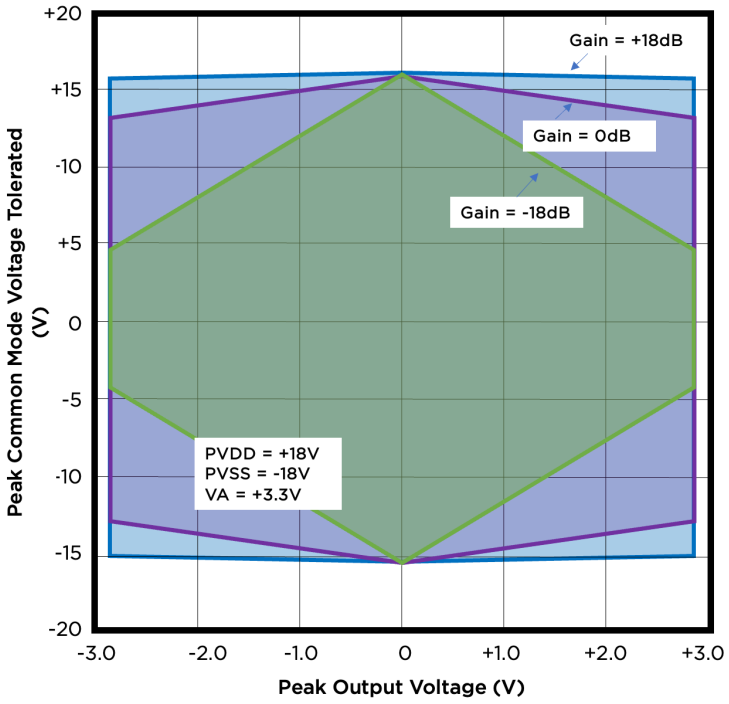


Figure 5: Common Mode Input Compliance vs. Output Voltage Swing. The TS5510 is capable of tolerating (and rejecting) over 8Vpp of CM input voltage while simultaneously driving 2Vrms differential output at any gain setting

Note that when powered from lower voltage rails (PVDD, PVSS) than shown in Figure 5, the "diamond" shape will collapse at high attenuation settings, where the input signal range cannot be accommodated by the Current Conveyor inputs. When powering PVDD, PVSS from +/-6V for instance, some of the highest attenuation settings will not be able to realize 2Vrms at the outputs. When higher voltage PVDD/PVSS are used however, the part can withstand and reject a very high level of CM interference whilst reproducing full scale differential signals simultaneously – across all gains settings - typically a known limitation of conventional Instrumentation Amplifier (INA) front end architectures.

7.2.4 RF Rejection

Not shown on the Application diagram, Radio Frequency filtering components should be considered to prevent high levels of out-of-band energy appearing on the TS5510 input pins. In extreme cases, the transistors used in the input circuit can demodulate sideband energy from strong RF carriers and unwanted noise or interference can appear in the audio domain as a result.

7.3 DC bias and operation

7.3.1 Common Mode O/P positioning

The output pins of each channel of the TS5510 can be positioned to optimally match the input requirements of the following ADC. This function is controlled by the CMLx pins. When left as a "no connect", internal resistors bias the common mode DC position on the output pins to one half that of the supply voltage VA. For instance, if VA = 3.3V, then the OUTxP and OUTxN pins would be biased up to 1.65V. It is recommended that a large value ceramic capacitor be connected from the each CMLx pin to AGND to prevent noise from corrupting the signal path.

The CMLx pins can be overridden by driving them from a low impedance voltage source; typically this would be derived from the VMID (or mid-voltage bias) of the ADC, meaning that the exact mid-point of the ADC will be asserted on the outputs of the TS5510, ensuring the differential output swing is centered on the ADC inputs. If this option is chosen, please note the limited voltage compliance of the CMLx pins (see Electrical Characteristics section for limits), also the effect of their input resistance having a loading effect on any applied voltage with significant source resistance.

7.3.2 Differential DC Control / Removal

While the TS5510 inputs are designed to be AC coupled, there are aspects of how DC is managed throughout the signal chain within the IC that are useful to understand when designing an audio capture system.

7.3.2.1 CGn capacitors

As higher gain settings are selected, the Current Conveyors (1st amplification stage) will build up small amounts of DC offset which end up being expressed across the Rg resistor chain (refer to Figure 4). As the 6dB gain boundaries are crossed as the gain is varied, this DC offset can lead to a transient that is amplified and manifests as an audible "click" on the output when a gain change is realized. To suppress this, the Rg chain (shown much simplified in Figure 4) is split internally and the mid-points are brought out to the CG pins (CGnP, CGnN). This allows the insertion of an AC coupling capacitor (330uF or higher recommended) which lowers the DC gain of the Current Conveyors (therefore minimizing DC offset) while still allowing high gains at audio band frequencies. These capacitors should be placed very close to the IC and any PCB routing to/from the pins minimized. High quality, low leakage capacitors should be used.

As no appreciable DC bias is expressed across these capacitors, low voltage polarized electrolytics can be used; bipolar capacitors will also work but are not necessary.

7.3.2.2 DC servo

As the output of the Current Conveyors are fed forward to the I to V (output) stage (referring again to Figure 4), this second stage is not subject to any common mode currents from the 1st stage, and only reacts to the differential currents that are fed forward. To ensure any DC offset from the either stage does not accumulate across the 2nd stage amp outputs (and end up causing audible clicks on gain changes), an internal DC servo circuit senses any differential DC across the OUTxP and OUTxN pins and injects a small DC corrective current back into the internal current summing node of the 2nd stage amplifier to remove it. The time constant of the servo is set by an internally trimmed transconductance stage current into the DCSx capacitors, which should be connected to AGND on each channel. With the values recommended, the DC servo loop corner is around 25mHz, well below the audio band. Note also that after power up and transitioning from SHUTDOWN mode, this long time constant will take some tens of seconds to settle out to its final value.

7.3.3 Output Drive Capability

The TS5510 outputs are designed to drive 2Vrms (or 3Vrms with VA = +5V) into an ADC input. Many contemporary ADCs use a sampled input which unfortunately require a large value capacitor across the ADC input pins. To ease the output load on the AFE (and to provide some anti-aliasing), series resistors are usually specified. The TS5510 has a strong output drive capability and can drive most available popular audio ADC input stages to full scale with minimal distortion and high slew rate.

7.4 Gain Control

7.4.1 Overview

The gains of each TS5510 input channel are set via the SPI interface. They can be set individually or applied to both channels at the same time. The default gain value (after power on or a RESET event) is 0dB. Unlike conventional Instrumentation Amplifier (INA) topologies, the TS5510 seamlessly transitions from gain to attenuation settings without using a resistive pad or divider on the input. The wide input range allows a 2Vrms output to be supported from an 8.9mVrms input (+47 dB gain setting) up to 8Vrms (-18dB gain setting, with suitable PVDD/PVSS), with 1dB increments available between these extremes.

7.4.2 Zero Cross Detection

Gain change SPI requests can be handled in one of two ways by the TS5510. One option is to have the new gain request have immediate effect on a valid write command. Consecutive writes (increasing or decreasing gains) can interact with any audio present in the channel, and can lead to “zipper noise”, or unwanted audio artefacts.

Enabling the Zero Cross Detection (ZCD) function in the TS5510 allows a signal dependent comparator to monitor the status of the signal in each channel; once a valid gain change is received, it holds off executing the gain change until a) there is no appreciable input signal or b) when any large signal reaches a mid-point (zero) crossing. In this way, the transient / step nature of the gain change is minimized.

This approach typically works well in the presence of channel signals that exhibit frequent “zero cross” events such as music, vocals, etc. In the presence of high level, low frequency tones, however, zero

cross events can be so infrequent that the gain change request is delayed too much before execution (so intermediate gain requests could be missed or perceived as delayed by the user). To offset this, a timeout function (per channel) forces the gain change after a predetermined time. This ZCD timeout is defined by a combination of external components (CTx capacitor value) and internal SPI register settings, allowing the exact setting to be optimized in the design.

The effect of enabling Zero Cross Detect (versus turned off) on requested gain changes is shown (using an example sequence) in Figure 6:

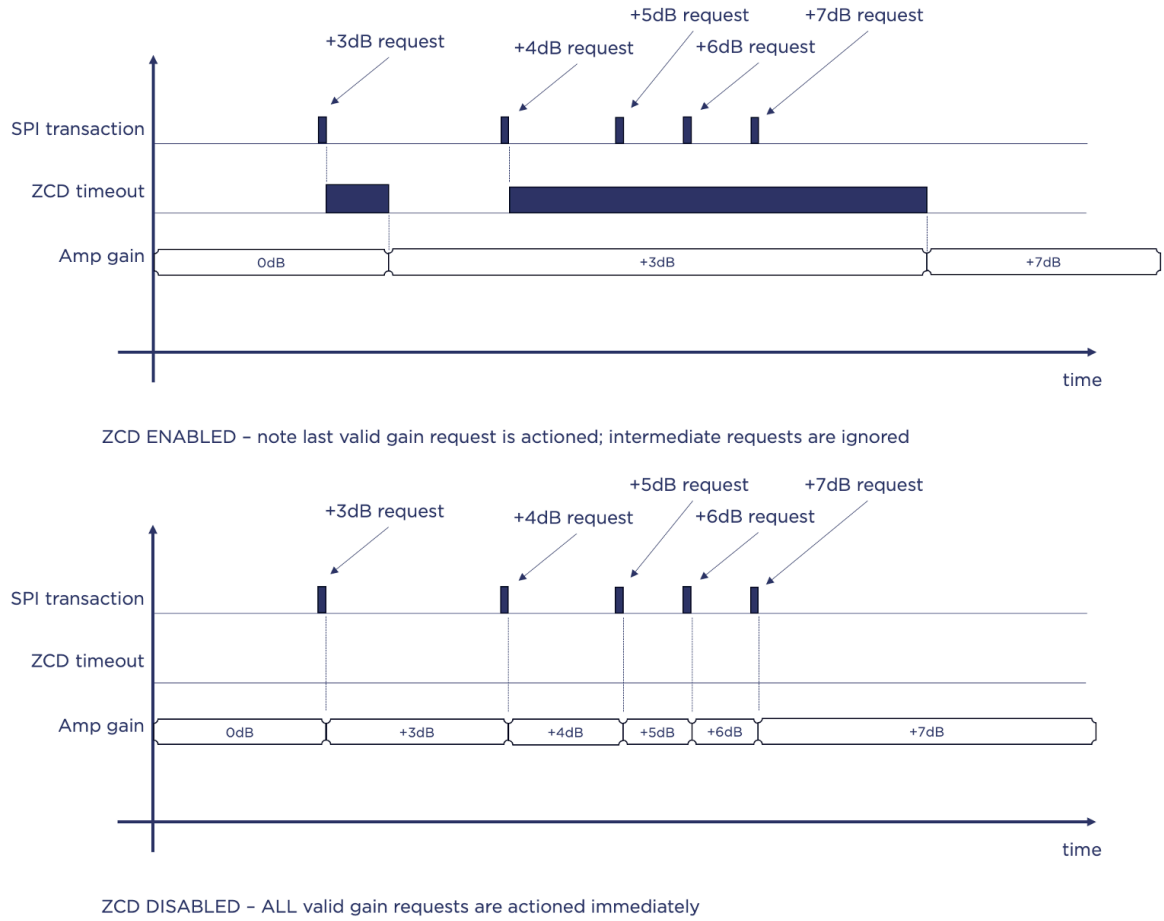


Figure 6: Simplified example of gain change execution with ZCD enabled & audio present in the channel (upper plot) and ZCD disabled (lower). Each channel has its own timeout and zero-cross comparison

8 SPI Control Interface

8.1 SPI Interface Description

Independent control of both channels of the TS5510 is provided by the SPI interface. The interface input and output logic levels are defined by the voltage applied to the VL pin. The SPI interface is designed to be flexible and can be configured for acting as a single SPI mode 0 Target device, or in a daisy-chain configuration where multiple TS5510s can be controlled from one SPI Controller.

CSN is the chip select signal, SCK is the control port bit clock, SDI is the input data line from the SPI Controller. SDO is the (optional) output data line back to the Host. Note that the SDO pin is an actively driven logic output at all times.

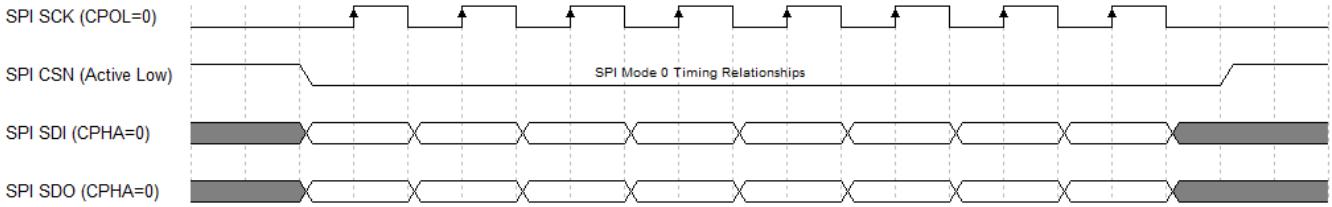


Figure 7: Basic clocking format for SPI Interface (mode 0 only)

8.2 Single TS5510 Example SPI Connection

Note that CSN and RSTN are active low.

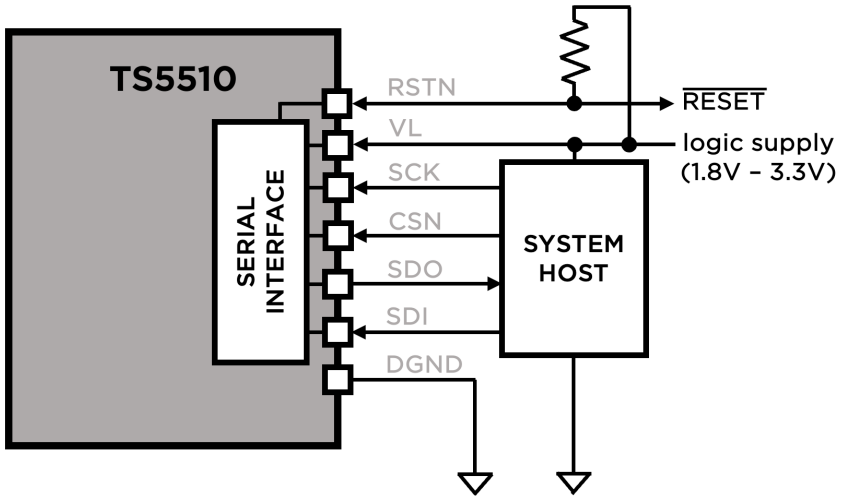


Figure 8: Single TS5510 (2 channel) interface connection

8.3 Multiple TS5510 Example SPI Connections

The TS5510 is designed to be used in either a standalone mode (2 channel system, see Figure 8), or for multi-channel audio systems, (4 or more audio channels) a "daisy-chain" SPI connection (see Figure 9). The daisy-chain connection ties up fewer SPI Controller physical lines than a parallel style connection, freeing up system resources and easing PCB routing.

Parallel SPI connections could be considered, but provision would have to be made for bringing in multiple SDO lines to the host, as all TS5510 SDO outputs would be active when operational. For a "Target write only" instantiation with no SDO readback, this approach is feasible. If reading back from the TS5510 array is desired, be aware that SDO does not enter a high impedance state when CSN is de-asserted when connecting these lines to the host.

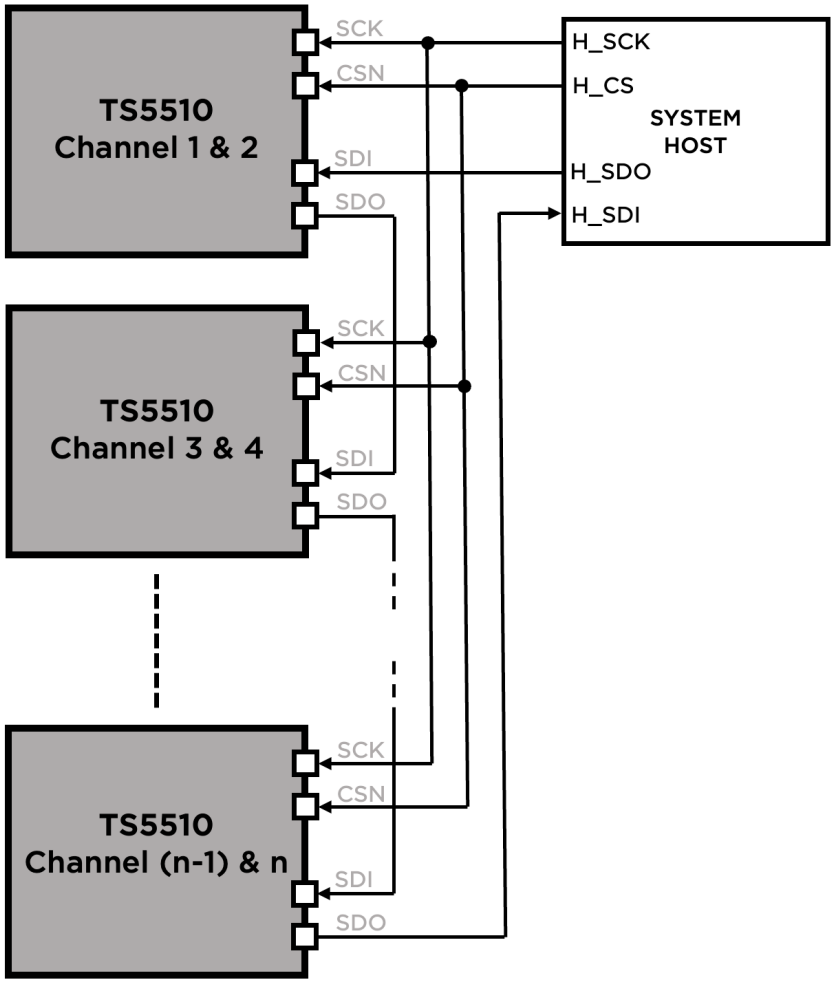


Figure 9: Connection for multiple TS5510s in a system, showing the "daisy-chain" connection for the data flow

Note the last device in the chain has its data optionally fed back to the System Host allowing register READ functionality.

8.4 Register SPI WRITE Sequence

Daisy-chained devices require SPI transactions of [Number of Devices x 16-bit] length, the header being the first byte transmitted followed by a payload byte of each daisy-chain packet. These are formatted such that first 16-bits transmitted by the host shall be processed by the device farthest away in the daisy-chain.

The outgoing (SDO) daisy-chain packets shall be formatted such that first 16-bits received by the host shall be generated by the closest device in the host's "incoming" SPI path. SPI packets shall be processed by all target devices on the rising edge of the SPI CSN. Typical WRITE command structure (single device) is shown below:

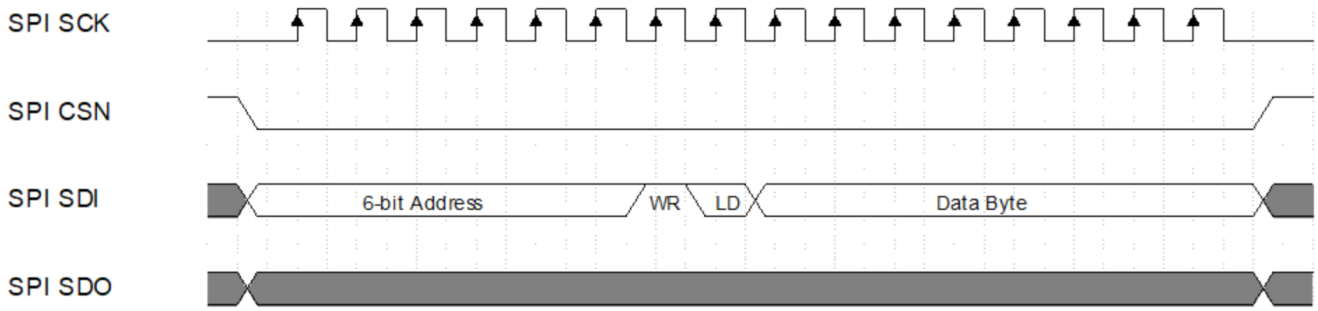


Figure 10: Basic WRITE command format

The LD bit is only relevant when writing to the MODE_CTRL or GAIN_CTRLx registers. It has no effect on other register writes. The settings allow for either single channel, unique values for each channel, or duplicate values to both channels. See also the sections on Gain Control and Mode Control Registers.

ZCD_DIS field	SPI LD bit	CMN_LOAD field	GAIN_CTRLx register	Description
X	0	0	ch1 or ch2	GAIN_CTRL1 and GAIN_CTRL2 registers can be written to (preloaded) but the gains do not take effect yet (LD bit is zero)
1	1	0	(preloaded data)	When the LD bit is set in the SPI command, values in the GAIN_CTRL1 and GAIN_CTRL2 registers are applied on the rising edge of CSN
1	1	1	ch1 and ch2	When the CMN_LOAD bit (*see Mode Control Register section*) is set, a write to either the GAIN_CTRL1 or the GAIN_CTRL2 register will duplicate that gain to both the GAIN_CTRL1 and GAIN_CTRL2 registers. If the LD bit is also set, the gains are applied on the rising edge of CSN
0	1	0	(preloaded data)	When the LD bit is set in the SPI command, values in the GAIN_CTRL1 and GAIN_CTRL2 registers are applied. ZCD being enabled means a zero cross event will control actual gain update timing, per channel
0	1	1	ch1 and ch2	CMN_LOAD bit set means a write to either channel 1 or 2 gain registers will duplicate gain setting in both. If the LD bit is also set, ZCD being enabled means a zero cross event will control actual gain update timing, per channel

Table 1: Gain update options

8.5 Register SPI READ Sequence

A READ sequence is performed by initiating a SPI WRITE transaction containing the address of the desired register to be read within the 6-bit Read Address field in the WRITE command. On asserting CSN again, the data from that register will be clocked out of SDO, with the payload byte delivered after 16 SCK clock cycles (see below):

8.5.1 Typical READ command structure (single device)

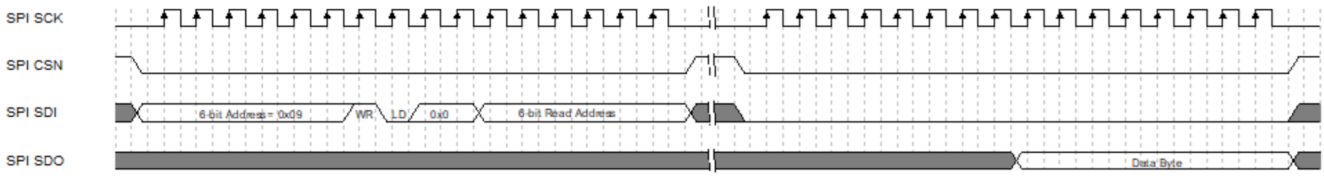


Figure 11: Basic READ command format

For daisy-chained devices, the above principle is just extended to accommodate the number of devices in the serial cascade. Multiple reads can be done in one transaction, attention should be paid to the sequencing of devices when setting up the READ, as to where the data from each TS5510 appears in the incoming vs. outgoing serial data. In Figure 12 below, which shows an example of two devices cascaded, note that the SDI sequence clocks out data for the farthest device (#2 in this example) first followed by device #1. The SDO data (as presented to the host) will see the #2 device from any previous READ command, followed by the device #1 payload byte. A further 32 clock cycle sequence (not shown) will be necessary to access the READ data addressed from the transaction requested in the below figure:

8.5.2 Typical READ / WRITE command structure (multiple devices)

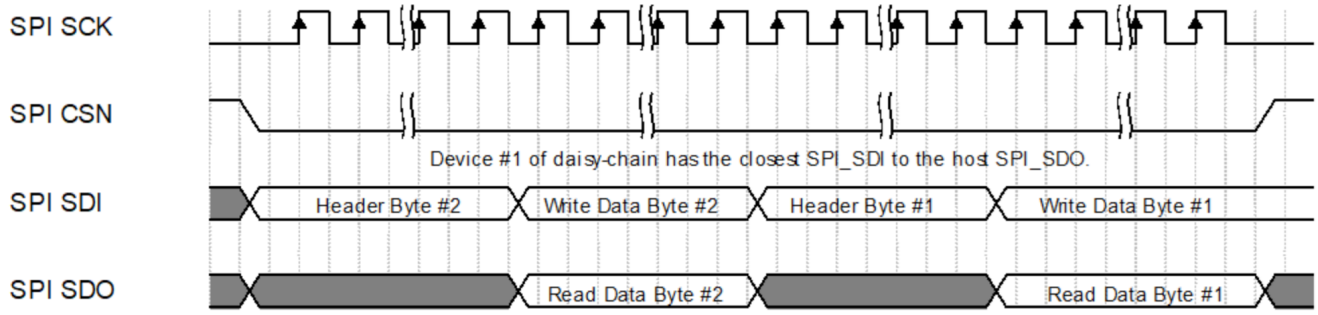


Figure 12: READ / WRITE command format example (2 devices shown)

8.6 Quick Reference

The table below shows the overall register map, names and access type (RW = Read/Write, or RO = Read Only), as well as power-on default values:

NAME	ADDRESS	R/W	DEFAULT	7	6	5	4	3	2	1	0
CHIP_ID	0x00	RO	0x05	PART [7:0]							
MODE_CTRL	0x01	RW	0x00	SHDN_AFE1	SHDN_AFE2	MUTE1	MUTE2	-	CMN_LOAD	-	-
GAIN_CTRL1	0x02	RW	0x00	SG1 [5:0]						SA1 [1:0]	
GAIN_CTRL2	0x03	RW	0x00	SG2 [5:0]						SA2 [1:0]	
GPIOA1	0x04	RW	0x20	A1IO	A1VAL	A1PUP	AZC_GPIO	-	-	-	-
GPIOA2	0x05	RW	0x20	A2IO	A2VAL	A2PUP	RSVD	-	-	-	-
GPIOB1	0x06	RW	0x20	B1IO	B1VAL	B1PUP	BZC_GPIO	-	-	-	-
GPIOB2	0x07	RW	0x20	B2IO	B2VAL	B2PUP	RSVD	-	-	-	-
ZCD_CTRL	0x08	RW	0x20	ZCD_DIS	-	ZCDT [2:0]			AZC_BUSY	BZC_BUSY	-
SPI_CTRL	0x09	RW	0x00	RSVD	-	SPI_READ[5:0]					
RSVD	0x0A	RW	0x80	-	-	-	-	-	-	-	-
SOFT_RESET	0x0B	RO	0x00	RESET_CMD[7:0]							

The following sections detail the individual register settings.

8.7 Register Description

8.7.1 Chip ID – address 0x00

Register Name	Address	Access	7	6	5	4	3	2	1	0
CHIP_ID	0x00	RO	PART [7:0]							
Default Values			0x05							

READ only (RO) address. This identifies / confirms the part as a TS5510. The value is 0x5.

8.7.2 Mode Control – address 0x01

Register Name	Address	Access	7	6	5	4	3	2	1	0
MODE_CTRL	0x01	RW	SHDN_AFE1	SHDN_AFE2	MUTE1	MUTE2	-	CMN_LOAD	-	-
Default Values			0	0	0	0	0	0	0	0

This register controls the major operational modes of the TS5510. The function can be READ or WRITE.

8.7.2.1 Shutdown control (bits 7:6)

Function: Writing a '1' to these bits puts the analog signal path and bias circuits into the lowest current shutdown mode. No audio is passed. The SPI interface will still be operational however, as will the GPIO functions. Default is '0', normal operation.

8.7.2.2 Mute bits (bits 5:4)

Function: Writing a '1' to these bits will set the analog channels to full attenuation or mute status. All bias and analog circuitry will be active, just not passing any meaningful signal. DC bias conditions are maintained. Default is '0', normal operation.

8.7.2.3 Common Load (bit 2)

Function: Setting to '1' enables auto-load feature of gain control fields which uses a common value for Channel 1 and 2. When set, writing to either GAIN_CTRL1 or GAIN_CTRL2 registers will update gain settings of both channels with the same values at the same time. Individual channels can be set individually, or preloaded with next required value when this is set to '0'.

8.7.3 Signal Gain & attenuation, channels 1 and 2 – address 0x02, 0x03

Register Name	Address	Access	7	6	5	4	3	2	1	0
GAIN_CTRL1	0x02	RW	SG1 [5:0]						SA1 [1:0]	
Default Values			0x00						0x0	
Register Name	**Address**	**Access**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GAIN_CTRL1	0x03	RW	SG2 [5:0]						SA2[1:0]	
Default Values			0x00						0x0	

These registers are identical, address 0x02 controls channel 1, 0x03 channel 2.

8.7.3.1 Signal Gain (bits 7:2)

Function: These bits set the requested positive gains, individually, for each channel. 5 bits cover the 0dB to +47dB gain range as described in the table below:

SGx[7:2] setting (binary)	Gain realized
000000	0dB
000001	1dB
000010	2dB
000011	3dB
::::::	::::::
101111	47dB
110000 and above	47dB

Table 2: Signal Gain set bits (individual channels)

Note that all SGx settings higher than 101111b all map to the highest gain setting (+47dB). When setting gains of 0dB and above, note that the SAx (attenuation) bits should be set to the default value of 0x00.

8.7.3.2 Signal Attenuation (bits 1:0)

Function: These bits set the coarse attenuation modes of the TS5510. Internally, that attenuation is achieved by a precision scaling down of the signal current fed forward from the 1st stage to the 2nd stage. Fine gain (1dB) precision is done by using the Signal Attenuation bits in conjunction with the first 5 settings of the Signal Gain bits (SGx) as outlined in the table below:

SAx[1:0] setting	SGx[7:2] setting	Gain Realized
00	000000	0dB
01	000101	-1dB
01	000100	-2dB
01	000011	-3dB
01	000010	-4dB
01	000001	-5dB
01	000000	-6dB
10	000101	-7dB
10	000100	-8dB
10	000011	-9dB
10	000010	-10dB
10	000001	-11dB
10	000000	-12dB
11	000101	-13dB
11	000100	-14dB
11	000011	-15dB
11	000010	-16dB
11	000001	-17dB
11	000000	-18dB

Table 3: Signal Attenuation set bits (individual channels)

Note that duplicate (but non-preferred) gain settings can be generated by incorrect setting of the signal gain (SGx) bits, when in attenuation modes. It is not recommended to use the TS5510 in this way. The settings as outlined in the above tables are the recommended for optimum performance.

8.7.4 GPIOs - address 0x04 through 0x07

The TS5510 General Purpose Input / Outputs (GPIOs) are designed to allow maximum flexibility in system control and function. There are two types of GPIO present on the device. The only difference is that two of the four GPIOs can be set to output the functional status of the associated channel zero cross detect (ZCD) counter function. The other type of GPIO (GPIOx2) cannot access this function.

Register Name	Address	Access	7	6	5	4	3	2	1	0
GPIOA1	0x04	RW	A1IO	A1VAL	A1PUP	AZC_GPIO	-	-	-	-
Default Values			0	0	1	0	0	0	0	0
Register Name	**Address**	**Access**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GPIOB1	0x06	RW	B1IO	B1VAL	B1PUP	BZC_GPIO	-	-	-	-
Default Values			0	0	1	0	0	0	0	0

8.7.4.1 GPIOx1 IO Direction Control (bit 7)

Function: Sets basic GPIO direction and function. Writing '0' sets it as an input (so the input pin logic level can be read by the SPI interface), '1' configures it as a logic output. Default (power up) value is an input, to prevent any possible contention in-system.

8.7.4.2 GPIOx1 Output Value (bit 6)

Function: When the GPIOx1 is set as an output, a WRITE to this bit will be reflected on the logic output. If the GPOIOx1 is configured as an input, the bit will reflect the logic value applied at the pin when the READ occurs. Note that the READ function can be overwritten by the setting of bit 4 (see later).

8.7.4.3 GPIOx1 Logic Pull-up Control (bit 5)

Function: If a '0' is written here, the internal weak pull up is disabled (if configured as a logic input). If configured as a logic output, this will set it to "open drain". If '1', then the internal (on chip) pull up is enabled in either case.

8.7.4.4 GPIOx1 ZCD Status Output (bit 4)

Function: This bit redirects the GPIO to reflect the current internal status of the associated ZCD circuitry – effectively a "ZCD busy" signal monitor for each channel. Logically, the output will be a function of:

GPIOA1 = 0x04[7] AND 0x04[4] AND 0x08[2] for channel 1

GPIOB1 = 0x06[7] AND 0x06[4] AND 0x08[1] for channel 2

Register Name	Address	Access	7	6	5	4	3	2	1	0
GPIOA2	0x05	RW	A2IO	A2VAL	A2PUP	RSVD	-	-	-	-
Default Values			0	0	1	0	0	0	0	0
Register Name	Address	Access	7	6	5	4	3	2	1	0
GPIOB2	0x07	RW	B2IO	B2VAL	B2PUP	RSVD	-	-	-	-
Default Values			0	0	1	0	0	0	0	0

8.7.4.5 GPIOx2 IO Direction Control (bit 7)

Function: Sets basic GPIO direction and function. Writing '0' sets it as an input (so the input pin logic level can be read by the SPI interface), '1' configures it as a logic output. Default (power up) value is an input, to prevent any possible contention in system.

8.7.4.6 GPIOx2 Value (bit 6)

Function: When the GPIOx2 is set as an output, a WRITE to this bit will be reflected on the logic output. If the GPOIOx2 is configured as an input, the bit will reflect the logic value applied at the pin when the READ occurs.

8.7.4.7 GPIOx2 Logic Pull-up Control (bit 5)

Function: If a '0' is written here, the internal weak pull up is disabled (if configured as a logic input). If configured as a logic output, this will set it to "open drain". If '1', then the internal (on chip) pull up is enabled in either case.

8.7.4.8 RSVD (bit 4)

Function: This bit is reserved. When writing to these registers, set this bit to a '0'.

8.7.5 ZCD (Zero Cross Detect) Control – address 0x08

This register controls the settings of the Zero Cross Detection feature of the TS5510.

Register Name	Address	Access	7	6	5	4	3	2	1	0
ZCD_CTRL	0x08	RW	ZCD_DIS	-	ZCDT [2:0]			AZC_BUSY	BZC_BUSY	-
Default Values			0	0	0x4			0	0	0

8.7.5.1 ZCD Disable (bit 7)

Function: This bit turns off the ZCD function of the gain switching, meaning gains will be switched on the receipt of a new gain command immediately. ZCD is enabled by default. Both channels are enabled / disabled together.

8.7.5.2 ZCD Timeout Duration (bits 5:3)

Function: These bits set the timeout period for a ZCD event. The range is user adjustable by writing to these bits from 4ms to 100ms. Default is 6.7ms. The timing of these may be further optimized by the user, by choosing a different value for the CTx capacitor, per channel. The timing for each setting is shown in the table below, and assumes a value for CTx of 100nF:

ZCDT(5:3) setting	ZCD timeout
000	100ms
001	25ms
010	12.5ms
011	9.1ms
100 (default)	6.7ms
101	5.6ms
110	4.5ms
111	4.0ms

Table 4: Nominal ZCD timeout settings (assumes CTx = 100nF)

8.7.5.3 ZCD Status (bits 1/2)

Function: These bits indicate the status of the ZCD at any given point. When a READ to this register is requested, the values of the ZCD operation for each channel are latched, and the result read out. A '1' indicates that a new gain request has been initiated, but the ZCD comparator is waiting for a zero crossing event to change to the new gain value. Bit 2 reports channel 1 status, bit 1 channel 2.

8.7.6 SPI Control – address 0x09

This register controls the settings of the SPI of the TS5510.

Register Name	Address	Access	7	6	5	4	3	2	1	0
SPI_CTRL	0x09	RW	RSVD	-	SPI_READ[5:0]					
Default Values			0	0	0x00					

8.7.6.1 RSVD (bit 7)

Function: This bit is reserved. When writing to this register, set this bit to a '0'.

8.7.6.2 SPI_READ (bits 5:0)

Function: These bits set the SPI transaction read address. This register value should be set prior to the respective SPI read transaction.

8.7.7 Soft Reset – address 0x0B

This register controls the digital soft reset of the TS5510.

Register Name	Address	Access	7	6	5	4	3	2	1	0
SOFT_RESET	0x0B	WO	RESET_CMD[7:0]							
Default Values			0x00							

8.7.7.1 Reset Command (bits 7:0)

Function: Soft reset control register. Writing a value of 0xA5 requests a reset of the digital domain. All registers values are set to default. All other values are reserved.

9 Applications and Design Considerations

9.1 Application Schematic

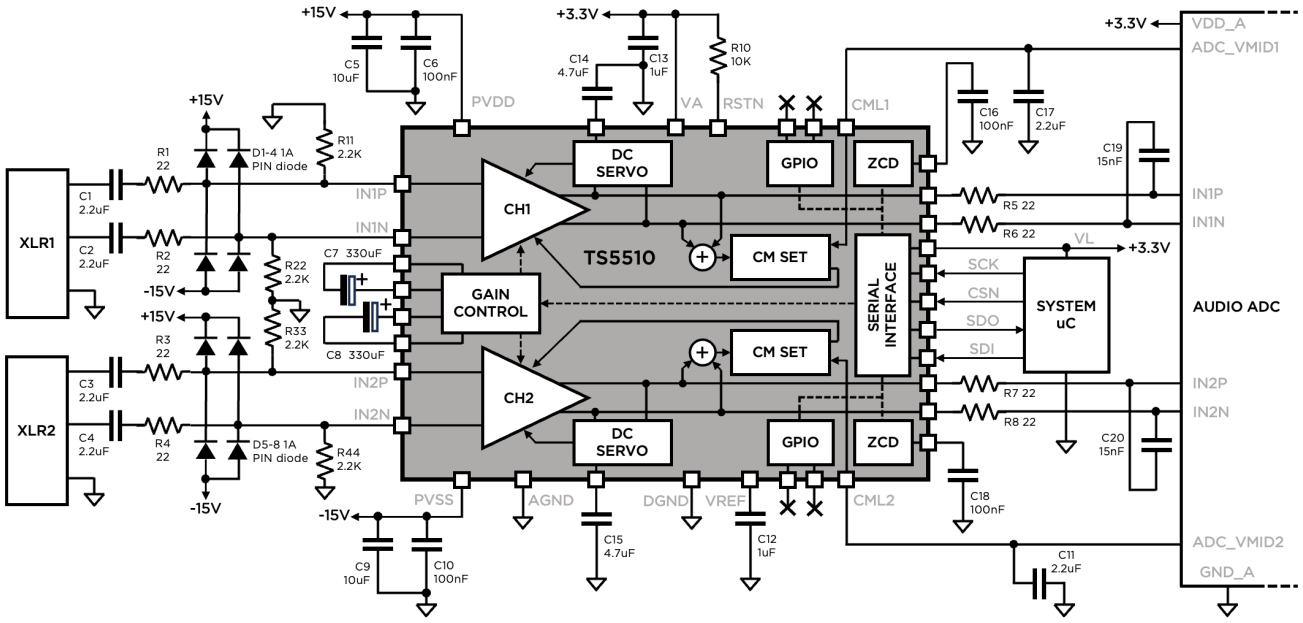


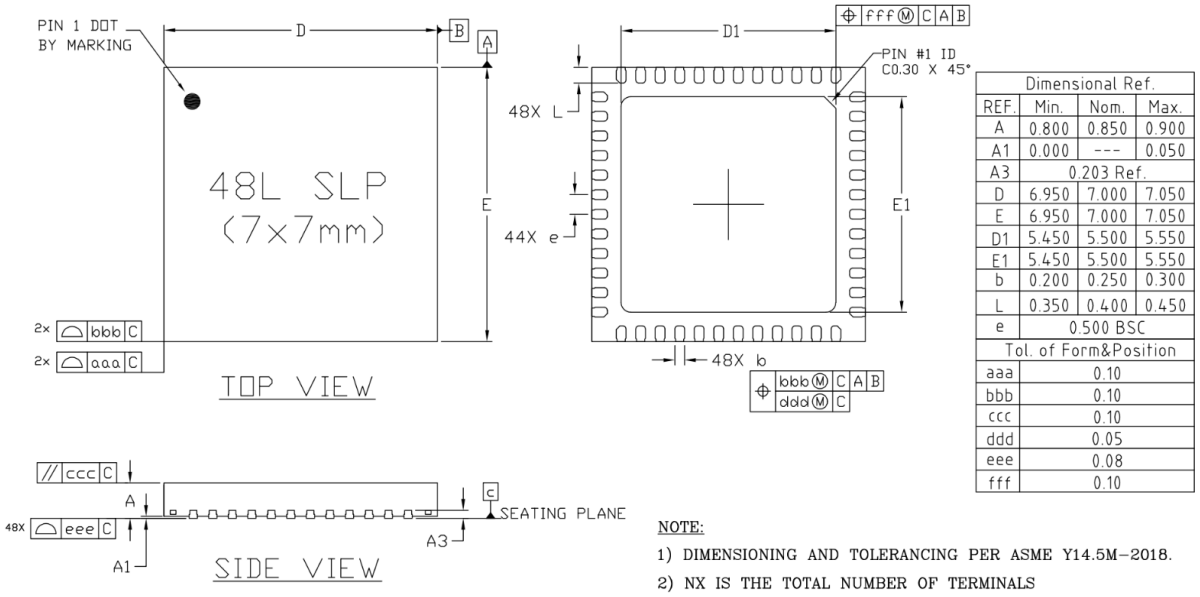
Figure 12: TS5510 Application Schematic

The above figure shows a typical application of the TS5510 as a stereo AFE for digitizing analog audio signals. The front end is AC coupled to the audio inputs (in this case, XLR types), with series protection resistors R1-R4 working with the input protection diodes D1-D8 to prevent excessive input transients damaging the device. PVDD/PVSS rails are set at +/-15V allowing a wide range of input signal amplitudes to be accommodated. The TS5510 outputs are biassed directly from the ADC VMID pins (decoupled by C11, C17) and directly coupled to the differential ADC inputs. Gain and mode control is supplied by the system uC or host, via the SPI connections shown.

10 Part Packaging Information

10.1 Package Drawing

TS5510 is packaged as a 48 pin QFN with a pin pitch of 0.5mm. It is nominally 7mm x 7mm in body size. Figure 12 shows the package outline drawing.



Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.800	0.850	0.900
A1	0.000	---	0.050
A3	0.203 Ref.		
D	6.950	7.000	7.050
E	6.950	7.000	7.050
D1	5.450	5.500	5.550
E1	5.450	5.500	5.550
b	0.200	0.250	0.300
L	0.350	0.400	0.450
e	0.500 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Figure 13: TS5510 QFN-48 Outline Drawing

10.2 Date Code

The manufacturing date code is printed on the package. The date code has the format of YYWW where YY is the last 2 digits of the manufacturing year, and WW is the week of manufacture in the year.

11 Pin List

#	Pin Name	Pin Type	Pin Description
1	CG1N	Analog	CG1 capacitor connection, negative
2, 11	PVSS	Supply	Negative power rail, input stage
3, 10, 18, 43	AGND	Supply	Analog GND connection (0V)
4	IN1P	Analog In	Ch 1 Analog input, positive phase
5	IN1N	Analog In	Ch 1 Analog input, negative phase
6, 15, 17, 25, 44, 46	NC	N/A	Do not connect
7	VREF	Analog	Internal reference. Connect 1uF to AGND
8	IN2P	Analog in	Ch 2 Analog input, positive phase
9	IN2N	Analog in	Ch 2 Analog input, negative phase
12	CG2P	Analog	CG2 capacitor connection, positive
13	CG2N	Analog	CG2 capacitor connection, negative
14, 47	PVDD	Supply	Positive power rail, input stage
16, 20, 41, 45	VA	Supply	Output stage power rail
19	DCS2	Analog	Ch 2 DC servo capacitor. Connect between DCS2 and AGND
21	OUT2P	Analog out	Ch 2 Analog output, positive phase
22	OUT2N	Analog out	Ch 2 Analog output, negative phase
23	CML2	Analog	Ch 2 Common mode reference (*see detailed description*)
24	CT2	Analog	ZCD timing, Ch 2. Connect 100nF to AGND

(continues...)

Pin List (continued)

#	Pin Name	Pin Type	Pin Description
26	GPIOB2	Digital	Assignable General Purpose I/O *(see detailed description)*
27	GPIOB1	Digital	Assignable General Purpose I/O *(see detailed description)*
28	DGND	Supply	Digital GND connection (0V)
29	SDI	Digital in	SPI interface Data Input
30	SDO	Digital out	SPI Interface Data Output
31	SCK	Digital in	SPI Clock Input
32	CSN	Digital in	SPI Chip Select (active low)
33	VL	Supply	Digital Circuit power rail and Logic I/O reference
34	GPIOA2	Digital	Assignable General Purpose I/O *(see detailed description)*
35	GPIOA1	Digital	Assignable General Purpose I/O *(see detailed description)*
36	RSTN	Digital	Reset, active LOW *(see detailed description)*
37	CT1	Analog	ZCD timing, Ch 1. Connect 100nF to AGND
38	CML1	Analog	Ch 1 Common mode reference (*see detailed description*)
39	OUT1P	Analog out	Ch 1 Analog output, positive phase
40	OUT1N	Analog out	Ch 1 Analog output, negative phase
42	DCS1	Analog	Ch 1 DC servo capacitor. Connect between DCS1 and AGND
48	CG1P	Analog	CG1 capacitor connection, positive
-	AGND	Supply	Exposed pad – connect to AGND

12 Mechanical, Packaging and Handling Information

Device	Package Type	Pins	Package Qty	RoHS Plan	Lead Finish	MSL Peak Temp	Op Temp (°C)	Storage Temp (°C)	Device Marking
TS5510	QFN48	48	-	RoHS & no Sb/Br	-	-	-40 to 85	-40 to 150	TS5510

12.1 Electrostatic Discharge Caution

TS5510 is an ESD sensitive device with an HBM rating of Class 1C (1000V) per JS-001-2017. The device should be placed in conductive foam during storage or handling to prevent damage due to electrostatic discharge. Refer to JESD625 for handling precautions.

12.2 MSL

TS5510 is an MSL3 device per J-STD-020. Refer to J-STD-033 for specific handling requirements and conditions.

12.3 Shelf Life

Shelf life is 12 months as per J-STD-033. Refer to J-STD-033 for additional shelf life information.

13 RoHS

TS5510 fully complies with the RoHS Directive 002/95/EC requirements without exemption and is Halogen-Free as defined by IEC 61249-2-21.

Revision History

Revision	Modifications	Modification Date
1.3	Initial release	January 19, 2026

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Triad Semiconductor
1760 Jonestown Road
Winston-Salem NC 27103
United States

info@triadsemi.com
sales@triadsemi.com

FAQ – help.triadsemi.com

phone: (336) 774-2150
fax: (336) 774-2140