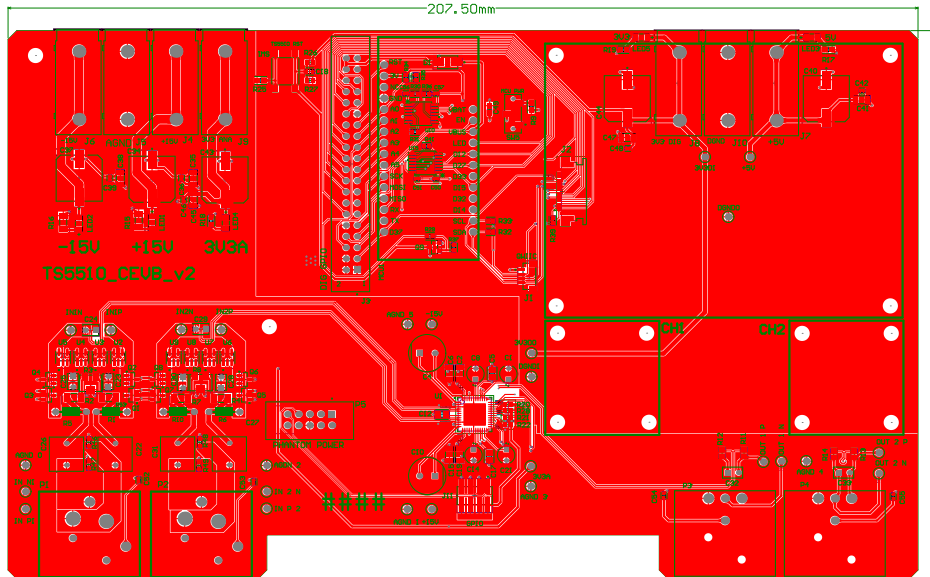


Layer	Name	Material	Thickness	Gerber
	Top Overlay			GTO
	Top Solder	Solder Resist	0.013mm	GTS
	Top Surface Finish	Nickel, Gold	0.004mm	
1	Top Layer		0.070mm	GTL
	Dielectric 1	PP-004	0.066mm	
2	GND0	CF-004	0.018mm	G1
	Dielectric 3	PP-004	0.066mm	
3	+15V	CF-004	0.018mm	G2
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	Dielectric 2	PP-004	0.066mm	
6	Bottom Layer		0.070mm	GBL
	Bottom Surface Finish	Nickel, Gold	0.004mm	
	Bottom Solder	Solder Resist	0.013mm	GBS
	Bottom Overlay			GBO

Total board thickness: 1.623mm



CONTACTS	PCB DESIGN	Insert Name	PH: Insert Number	insertname@triadsemi.com
	ENGINEERING	Insert Name	PH: Insert Number	insertname@triadsemi.com

NOTE: SUPPLIER MUST SEND EMAIL TO ABOVE LISTED CONTACTS IF JOB IS PLACED ON HOLD

FABRICATION NOTES:

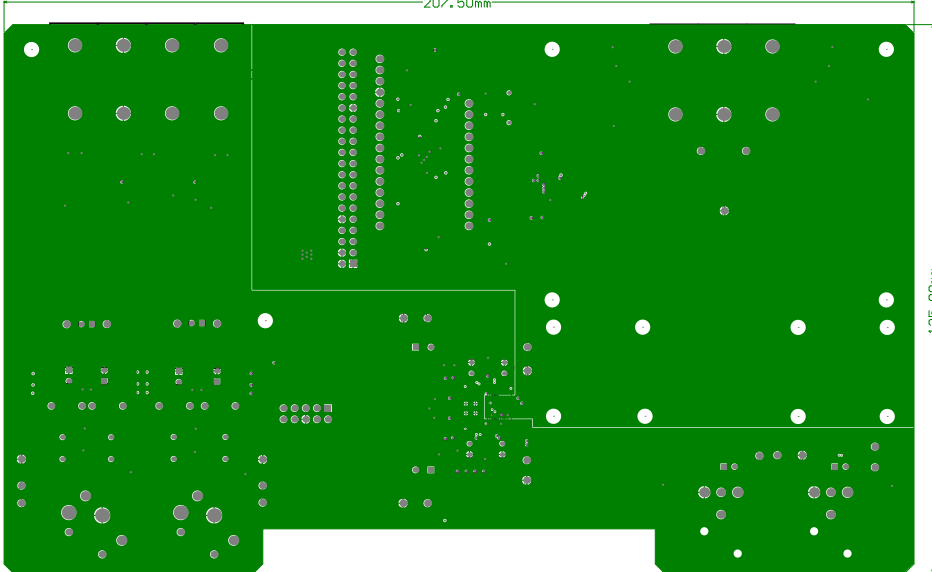
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☐ ELECTRO-PLATED HARD GOLD ☐ ELECTRO-PLATED SOFT GOLD
- SOLDERMASK SHALL BE LIQUID PHOTO-IMAGEABLE, Blue, GLOSSY.
- SILKSCREEN SHALL BE HIGH TEMPERATURE, NON-CONDUCTIVE, WHITE EPOXY BASED INK.
- THE PCB SHALL BE MARKED WITH BOTH THE FABRICATOR'S NAME OR LOGO AND A DATE CODE SHOWING CALENDAR YEAR AND WEEK (YY/WW).
- 100% ELECTRICAL TEST: ☐ GERBER EXTRACTED NETLIST
☒ IPC-D-356 FORMAT
☐ NO E.T.
- Place serialization number on each board Top silk (### Location) starting at 001 and increment by 1.
- CONTROLLED IMPEDANCE: ☐ YES ☒ NO
* DIELECTRIC(S) THAT CAN BE ADJUSTED TO OBTAIN FINISHED THICKNESS: LAYERS 3-4
* GERBER DATA SUPPLIED WITH DESIRED FINAL TRACE WIDTHS. PROCESS COMPENSATION TRACE WIDTH ADJUSTMENT TO BE DONE BY PCB FABRICATOR.
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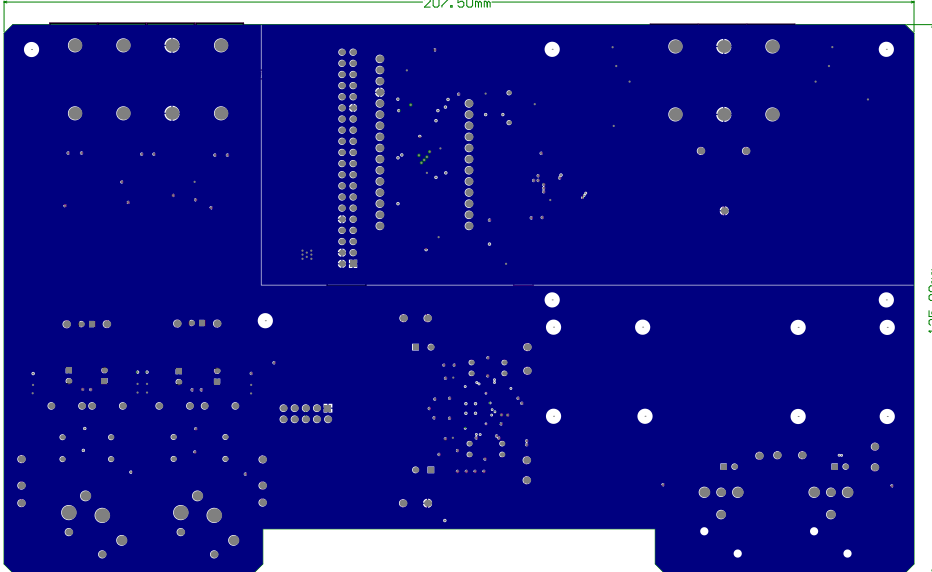
TRIADSEMI ASSEMBLY NOTES:

- ☒ WORKMANSHIP & SOLDER PER PC-A-610C, CLASS 2
- ☒ PLACE S/N LABEL IN SPACE INDICATED (IF APPLICABLE)

TITLE: TS5510 Customer Eval Board Layout			
PCB PROJECT NAME: TS5510_CEUVB	ORG/DEPT: TriadSemi/Lab	DATE: 12/15/2025	
PCB DOCUMENT FILE NAME: TS5510_CEUVB_v2.PcbDoc	DRAWN BY:	SHEET SIZE: B	SHEET N: 2
DOCUMENT NUMBER: TS5510_CEUVB	REVISION: 2	ALL DIMENSIONS IN INCHES UNLESS OTHERWISE SPECIFIED SCALE: 0.5X	

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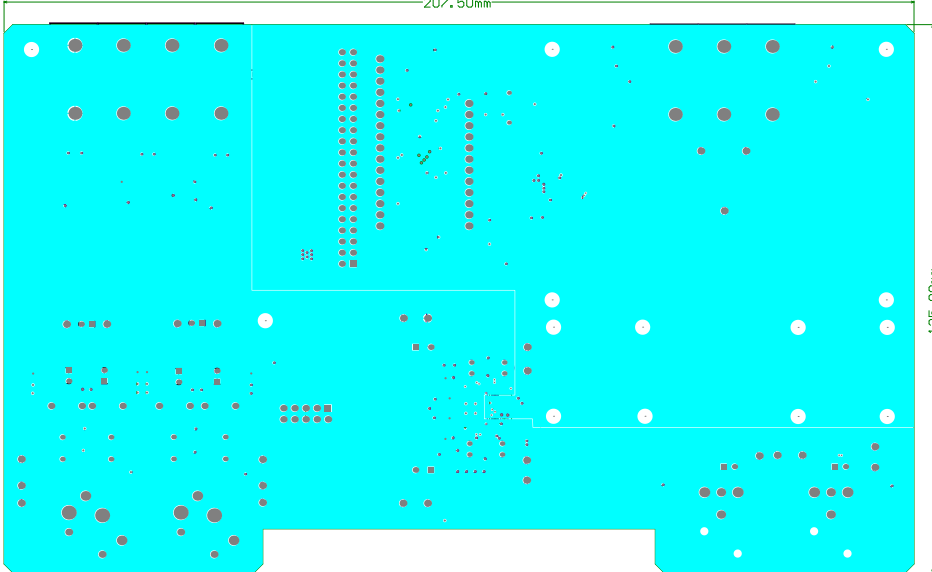
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☐ ELECTRO-PLATED HARD GOLD ☐ ELECTRO-PLATED SOFT GOLD
4. SOLDERMASK SHALL BE LIQUID PHOTO-IMAGEABLE, Blue, GLOSSY.
5. SILKSCREEN SHALL BE HIGH TEMPERATURE, NON-CONDUCTIVE, WHITE EPOXY BASED INK.
6. THE PCB SHALL BE MARKED WITH BOTH THE FABRICATOR'S NAME OR LOGO AND A DATE CODE SHOWING CALENDAR YEAR AND WEEK (YY/WW).
7. 100% ELECTRICAL TEST: ☐ GERBER EXTRACTED NETLIST
☒ IPC-D-356 FORMAT
☐ NO E.T.
8. Place serialization number on each board Top silk (### Location) starting at 001 and increment by 1.
9. CONTROLLED IMPEDANCE: ☐ YES ☒ NO
* DIELECTRIC(S) THAT CAN BE ADJUSTED TO OBTAIN FINISHED THICKNESS: LAYERS 3-4
* GERBER DATA SUPPLIED WITH DESIRED FINAL TRACE WIDTHS. PROCESS COMPENSATION TRACE WIDTH ADJUSTMENT TO BE DONE BY PCB FABRICATOR.
10. VIA TYPES/ASSOCIATED LAYERS: THRU-HOLE LAYER1-6

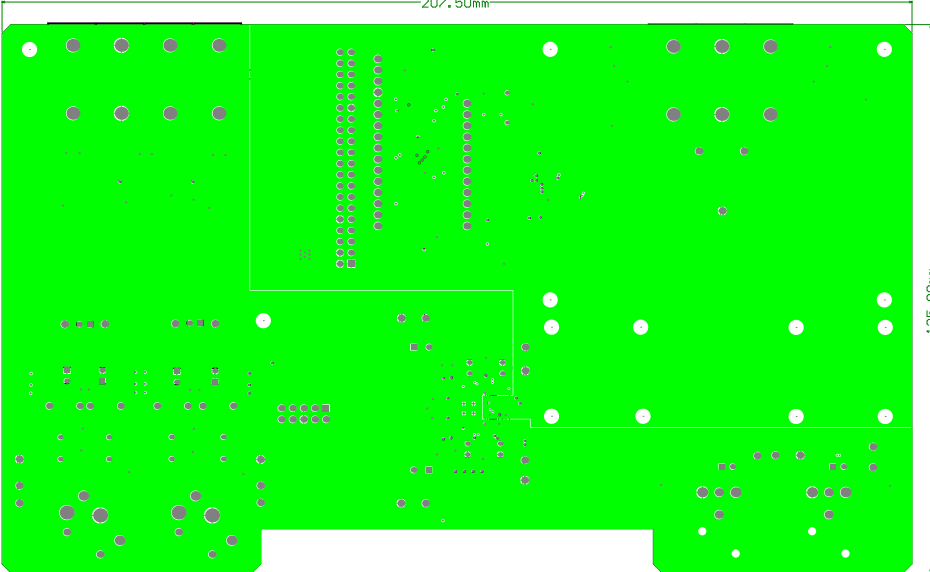
TRIADSEMI ASSEMBLY NOTES:

- ☒ WORKMANSHIP & SOLDER PER PC-A-610C, CLASS 2.
- ☒ PLACE S/N LABEL IN SPACE INDICATED (IF APPLICABLE)

TITLE: TS5510 Customer Eval Board Layout			
PCB PROJECT NAME: TS5510_CEUVB		ORG/DEPT: TriadSemi/Lab	DATE: 12/15/2025
PCB DOCUMENT FILE NAME: TS5510_CEUVB_v2.PcbDoc		DRAWN BY: B	SHEET SIZE: 11x17 SHEET NO: 2
DOCUMENT NUMBER: TS5510_CEUVB		REVISION: 2	ALL DIMENSIONS IN INCHES UNLESS OTHERWISE SPECIFIED SCALE: 0.50



Triad Semiconductor, Inc.
1760 Jonestown Rd
Winston Salem, NC 27103
Phone: 336-774-2150
www.triadsemi.com

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CONTACTS		PCB DESIGN		Insert Name		PH: Insert Number		insertname@triadsemi.com																																																																																																	
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 **TRIAD**
SEMICONDUCTOR

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